

# Specifications

**PC-CARD-DAS16/16AO**



**MEASUREMENT  
COMPUTING™**

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# Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

## Analog input

Table 1. Analog input specifications

A/D converter type	AD976A
Resolution	16 bits
Number of channels	16 single-ended / 8 differential, software selectable
Input ranges	$\pm 10$ V, $\pm 5$ V, $\pm 2.5$ V, $\pm 1.25$ V, software programmable
A/D pacing (software programmable)	<ul style="list-style-type: none"><li>▪ Internal counter - 82C54</li><li>▪ External source - A/D External Pacer, software programmable for rising or falling edge</li><li>▪ Software polled</li></ul>
A/D trigger sources	External edge trigger (A/D External Trigger)
A/D triggering modes	Rising or falling edge trigger - software selectable
A/D gate sources	A/D External Trigger, gate high or low, software selectable A/D Pacer Gate, gate high
Burst mode	Software selectable option, burst rate = 100 kHz
Data transfer	From 4 k sample FIFO via REPINSW Programmed I/O
<i>A/D conversion time</i>	<i>5 <math>\mu</math>s max</i>
Calibrated throughput	200 kHz single channel, 100 kHz multiple channel. Minimum system requirement is Pentium II, 400 MHz.
Calibration	Auto-calibration, calibration factors for each range stored on board in nonvolatile RAM

## Accuracy

Accuracies are listed for a 200 kHz sampling rate, single channel operation, a 60 minute warm-up, and operational temperatures within  $\pm 2$  °C of internal calibration temperature. The calibrator test source high side is tied to Channel 0 In, and the low side tied to AGND.

Table 2. Absolute Accuracy specifications

Range	Absolute accuracy
$\pm 10.00$ V	$\pm 5.0$ LSB max
$\pm 5.000$ V	$\pm 5.0$ LSB max
$\pm 2.500$ V	$\pm 5.0$ LSB max
$\pm 1.250$ V	$\pm 5.0$ LSB max

Each PC-CARD-DAS16/16AO is tested at the factory to assure the board's overall error does not exceed accuracy limits described in Table 2.

Table 3. Calibrated accuracy specifications

Range	Gain Error	Offset Error	DLE (Note 1)	ILE (Note 1)
±10.00 V	±3 max	±1.5 max	-1.0, +1.75 max	±2.0 max
±5.000 V	±3 max	±1.5 max	-1.0, +1.75 max	±2.0 max
±2.500 V	±3 max	±1.5 max	-1.0, +1.75 max	±2.0 max
±1.250 V	±3 max	±1.5 max	-1.0, +1.75 max	±2.0 max

**Note 1:** These are the intrinsic specifications of the ADC. Software calibration may introduce a small additional amount of linearity error.

As shown in Table 3, total board error is a combination of gain, offset, differential linearity and integral linearity error. The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case errors are realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction.

Analog input full-scale gain drift	±0.60 LSB/°C max
Analog input zero drift	±0.15 LSB/°C max
Overall analog input drift	±0.75 LSB/°C max
Common mode range	±10 V min
CMRR @ 60 Hz	-76 dB min
Input leakage current	±20 nA max
Input impedance	10 MOhms min
Absolute maximum input voltage	+55/-40 V (fault protected via input mux)

## Crosstalk

Crosstalk is defined here as the influence of one channel upon another when scanning two channels at the maximum rate. A full scale 100 Hz triangle wave is input on channel 1; channel 0 is tied to analog ground at the connector. The table below summarizes the influence of channel 1 on channel 0 with the effects of noise removed. The residue on channel zero is described in LSB's.

Table 4. Channel to channel crosstalk specifications

Condition	Crosstalk	Per channel Rate	ADC Rate
±10.00 V	5LSB <sub>pk-pk</sub>	50 kHz	100 kHz
±5.000 V	6LSB <sub>pk-pk</sub>	50 kHz	100 kHz
±2.500 V	7LSB <sub>pk-pk</sub>	50 kHz	100 kHz
±1.250 V	10LSB <sub>pk-pk</sub>	50 kHz	100 kHz

## Noise performance

Table 5 summarizes the noise performance for the PC-CARD-DAS16/16AO. Noise distribution is determined by gathering 50K samples at 200 kHz with inputs tied to ground at the user connector.

Table 5. Noise performance specifications

Range	% within ±2 LSBs	% within ±1 LSB	Typical LSB <sub>rms</sub> *	Max LSB <sub>rms</sub> *
All ranges	78%	47%	1.8	4.7

\* RMS noise is defined as the peak-to-peak bin spread divided by 6.6.

## Analog output

Table 6. Analog output specifications

D/A converter type	LTC1655
Resolution	16 bits
Number of channels	2
Configuration	Voltage output, single-ended
Output range	$\pm 10$ V
D/A pacing	Software
Data transfer	Programmed I/O
Throughput	System dependent. Using the Universal Library programmed output function ( <code>cbAOut</code> ) in a loop in Visual Basic, a typical update rate of 1.5 kHz ( $\pm 200$ Hz) can be expected. The rate was measured on a 400 MHz Pentium II based PC.

## Accuracy

Table 7. Accuracy specifications

Absolute accuracy	$\pm 12.0$ LSB worst case error
Typical accuracy	$\pm 10.0$ LSB worst case error

Table 8. Calibrated accuracy components

Gain error	$\pm 3.0$ LSB max, $\pm 1.0$ LSB typ
Offset error	$\pm 1.5$ LSB max, $\pm 0.5$ LSB typ
Integral linearity error	$\pm 20.0$ LSB max, $\pm 8.0$ LSB typ
<i>Differential linearity error</i>	<i><math>\pm 1.0</math> LSB max, <math>\pm 0.3</math> LSB typ</i>

Each PC-CARD-DAS16/16AO is tested at the factory to assure the board's overall error does not exceed  $\pm 12.0$  LSB.

Total board error is a combination of gain, offset, integral linearity and differential linearity error. The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction. Although an examination of the chart and a summation of the maximum theoretical errors shows that the board could theoretically exhibit a  $\pm 25.5$  LSB error, our testing assures this error is never realized in a board that we ship.

Typical accuracy is derived directly from the various component typical errors. This typical, maximum error calculation for the PC-CARD-DAS16/16AO yields  $\pm 10.0$  LSB. However, this again assumes that each of the errors contributes in the same direction and the  $\pm 10.0$  LSB specification is quite conservative.

<i>Monotonicity</i>	<i>Guaranteed monotonic over temperature</i>
Analog output full-scale gain drift	$\pm 5.0$ LSB/ $^{\circ}$ C max
Analog output zero drift	$\pm 0.5$ LSB/ $^{\circ}$ C max
Overall analog output drift	$\pm 5.5$ LSB/ $^{\circ}$ C max
Slew rate	$\pm 0.7$ V/ $\mu$ s min
Current drive	$\pm 2$ mA min
<i>Output short-circuit duration</i>	<i>Indefinite @ 12 mA</i>
Output coupling	DC
Output impedance	0.1 ohms max

Miscellaneous	Double buffered output latches
	Coding: Offset Binary (0 code = -FS, 65535 code = +FS)
	Output voltage on power up and reset: -10 V (-FS)

## Digital input/output

Table 9. DIO specifications

Digital type	FPGA
Number of I/O	4
Configuration	One port, programmable 4 input or 4 output
Input low voltage	0.8 V max
Input high voltage	2.0 V min
Output low voltage (IOL = 4 mA)	0.32 V max
Output high voltage (IOH = -4 mA)	3.86 V min
<i>Absolute maximum input voltage</i>	<i>-0.5 V, +5.5 V</i>
Power-up / reset state	Input mode (high impedance)

## Interrupt

Table 10. Interrupt specifications

Interrupts	Programmable: Levels 2 – 15
Interrupt enable	Programmable. Default = disabled.
Interrupt sources	External (External Interrupt)
	A/D End-of-channel-scan
	A/D FIFO-not-empty
	A/D FIFO-half-full
	A/D Pacer

## Counter

Table 11. Counter specifications

Counter type	82C54
Configuration	3 down counters, 16 bits each
<b>Counter 1</b> - User counter	Source: Programmable external (Ctr 1 Clk) or 100 kHz internal source
	Gate: Available at connector (Ctr 1 Gate), pulled to logic high via 10K resistor (See Note 2)
	Output: Available at connector (Ctr 1 Out)
<b>Counter 2</b> - ADC Pacer Lower Divider	Source: Programmable, 1MHz or 10 MHz internal source
	Gate: Available at connector (A/D Pacer Gate), pulled to logic high via 10K resistor.
	Output: Chained to Counter 3 Clock
<b>Counter 3</b> - ADC Pacer Upper Divider	Source: Counter 2 Output
	Gate: Internal
	Output: Programmable as ADC Pacer clock. Available at user connector (ADC Pacer out)
<i>Clock input frequency</i>	<i>10 MHz max</i>
<i>High pulse width (clock input)</i>	<i>30 ns min</i>
<i>Low pulse width (clock input)</i>	<i>50 ns min</i>
<i>Gate width high</i>	<i>50 ns min</i>
<i>Gate width low</i>	<i>50 ns min</i>
<i>Input low voltage</i>	<i>0.8 V max</i>
<i>Input high voltage</i>	<i>2.0 V min</i>
<i>Output low voltage</i>	<i>0.4 V max</i>
<i>Output high voltage</i>	<i>3.0 V min</i>
Crystal oscillator frequency	10 MHz
Frequency accuracy	50 ppm

**Note 2:** If you are not driving the gate of User Counter 1, it is strongly recommended that it be connected to +5V (VDD).

## Power consumption

Table 12. Power consumption specifications

5V quiescent	150 mA typical, 170 mA max
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## Miscellaneous

Table 13. Miscellaneous specifications

+5 Volts	Available at I/O connector (+5V Power)
	Protected by resettable fuse:
	Hold current: 350 mA max @ 20 °C still air
	Trip current: 700 mA min @ 20 °C still air
	<i>Trip and recovery time:</i> 100 mS max
	On resistance: 1.3 Ohms max

## Environmental

Table 14. Environmental specifications

Operating temperature range	0 to 70 °C
Storage temperature range	-40 to 100 °C
Humidity	0 to 95% non-condensing

## Mechanical

Table 15. Mechanical specifications

Card dimensions	PCMCIA type II: 85.6 mm (L) x 54.0 mm (W) x 5.0 mm (H)
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## Connector and pin out

Table 16. Connector specifications

Connector type	50-pin connector
Compatible cables	CPCC-50F-39: 50-pin Micro connector to 50-pin female IDC, one-meter cable (39 inches).
	CPCC-50M-4: 50-pin Micro connector to 50-pin male IDC, 4 inch adapter cable. and C50FF-x: 50-pin IDC female to female cable. x = length in feet.
Compatible accessory products	CIO-MINI50 SCB-50

Table 17. 8-channel Differential mode pin out

Pin	Signal Name	Pin	Signal Name
1	AGND	26	DGND
2	CH0 HI	27	DIO0
3	CH0 LO	28	DIO1
4	CH1 HI	29	DIO2
5	CH1 LO	30	DIO3
6	CH2 HI	31	NC
7	CH2 LO	32	NC
8	CH3 HI	33	NC
9	CH3 LO	34	NC
10	CH4 HI	35	DA GND0
11	CH4 LO	36	DA OUT0
12	CH5 HI	37	DA GND1
13	CH5 LO	38	DA OUT1
14	CH6 HI	39	CTR1 CLK
15	CH6 LO	40	CTR1 GATE
16	CH7 HI	41	CTR1 OUT
17	CH7 LO	42	A/D EXTERNAL PACER
18	AGND	43	EXTERNAL INTERRUPT
19	N/C	44	A/D PACER GATE
20	N/C	45	A/D EXTERNAL TRIGGER
21	N/C	46	N/C
22	N/C	47	A/D PACER OUT
23	N/C	48	VDD +5V POWER
24	N/C	49	N/C
25	N/C	50	DGND

Table 18. 16-channel Single-ended mode pin out

Pin	Signal Name	Pin	Signal Name
1	AGND	26	DGND
2	CH0 IN	27	DIO0
3	CH8 IN	28	DIO1
4	CH1 IN	29	DIO2
5	CH9 IN	30	DIO3
6	CH2 IN	31	NC
7	CH10 IN	32	NC
8	CH3 IN	33	NC
9	CH11IN	34	NC
10	CH4 IN	35	DA GND0
11	CH12 IN	36	DA OUT0
12	CH5 IN	37	DA GND1
13	CH13 IN	38	DA OUT1
14	CH6 IN	39	CTR1 CLK
15	CH14 IN	40	CTR1 GATE
16	CH7 IN	41	CTR1 OUT
17	CH15 IN	42	A/D EXTERNAL PACER
18	AGND	43	EXTERNAL INTERRUPT
19	N/C	44	A/D PACER GATE
20	N/C	45	A/D EXTERNAL TRIGGER
21	N/C	46	N/C
22	N/C	47	A/D PACER OUT
23	N/C	48	VDD +5V POWER
24	N/C	49	N/C
25	N/C	50	DGND



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